Features

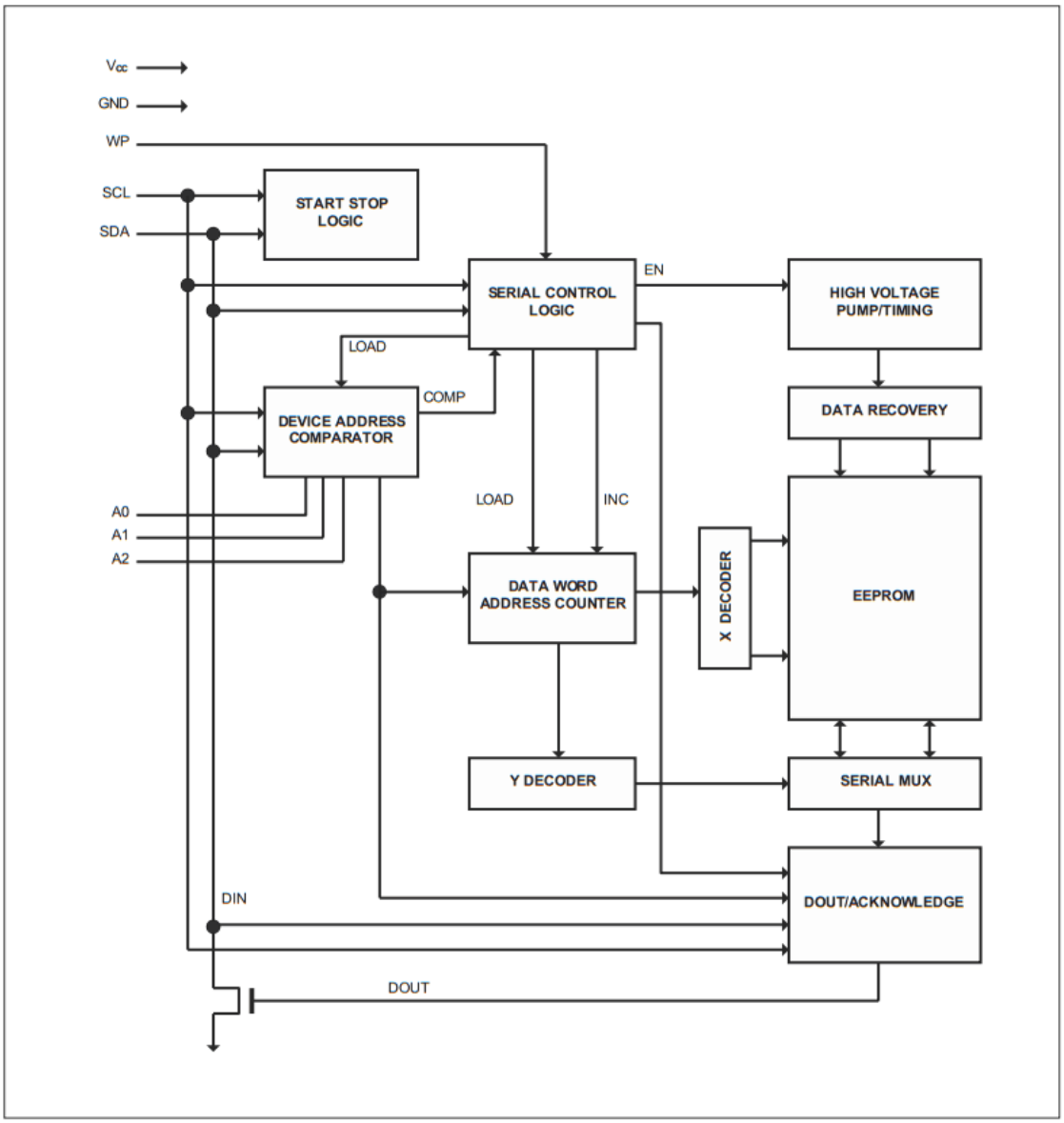
- Wide Voltage Operation
  VCC = 1.7V to 5.5V
- Operating Ambient Temperature:
  -40℃ to +85 ℃
- Internally Organized:
  - TX24C128, 16,384 X 8 (128K bits)
  - TX24C256, 32,768 X 8 (256K bits)
  - TX24C512, 65,536 X 8 (512K bits)
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1 MHz (5V), 400 KHz (1.7V , 2.5V, 2.7V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 64-byte Page (128K, 256K), 128-byte (512K) Write Modes
- Partial Page Writes Allowed
- Self-timed Write Cycle (5 ms max)
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- 8-lead PDIP/SOP/TSSOP packages

General Description

The TX24C128/TX24C256/TX24C512 provides 131,072/262,144/524,288 bits of serial electrically erasable and programmable read-only memory (EEPROM), organized as 16,384/32,768/65,536 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

The TX24C128/TX24C256/TX24C512 is available in space-saving 8-lead PDIP, 8-lead SOP, and 8-lead TSSOP packages and is accessed via a two-wire serial interface. In addition, the TX24C128/TX24C256/TX24C512 is available in 1.7V (1.7V to 5.5V) version.

Block Diagram



Pin Configuration

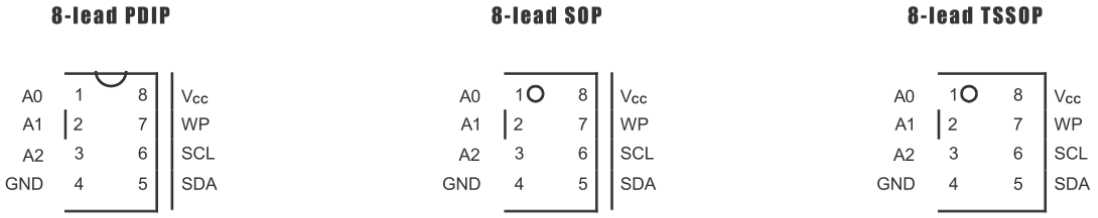


Table 1: Pin Configuration

Pin Name	Type	Functions
A0 - A2	I	Address Inputs
SDA	I/O & Open-drain	Serial Data
SCL	I	Serial Clock Input
WP	I	Write Protect
GND	P	Ground
VCC	P	Power Supply

Pin Descriptions

DEVICE/PAGE ADDRESSES (A2, A1 and A0): The A2, A1 and A0 pins are device address inputs that are hard wire for the TX24C128/TX24C256/TX24C512. Eight 128K/256K/512K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-O Red with any number of other open-drain or open-collector devices.

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

WRITE PROTECT (WP): The TX24C128/TX24C256/TX24C512 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protection pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following Table 2.

Table 2: Write Protect

WP Pin Status	Part of the Array Protected		
	TX24C128	TX24C256	TX24C512
At V_{CC}	Full (128K) Array	Full (256K) Array	Full (512K) Array
At GND	Normal Read / Write Operations		

Memory Organization

TX24C128, 128K SERIAL EEPROM: Internally organized with 256 pages of 64 bytes each, the 128K requires an 14-bit data word address for random word addressing.

TX24C256, 256K SERIAL EEPROM: Internally organized with 512 pages of 64 bytes each, the 256K requires an 15-bit data word address for random word addressing.

TX24C512, 512K SERIAL EEPROM: Internally organized with 512 pages of 128 bytes each, the 512K requires an 16-bit data word address for random word addressing.

Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 1 on page 5). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 2 on page 5).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 3 on page 5).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The TX24C128/TX24C256/TX24C512 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition.

Figure 1: Data Validity

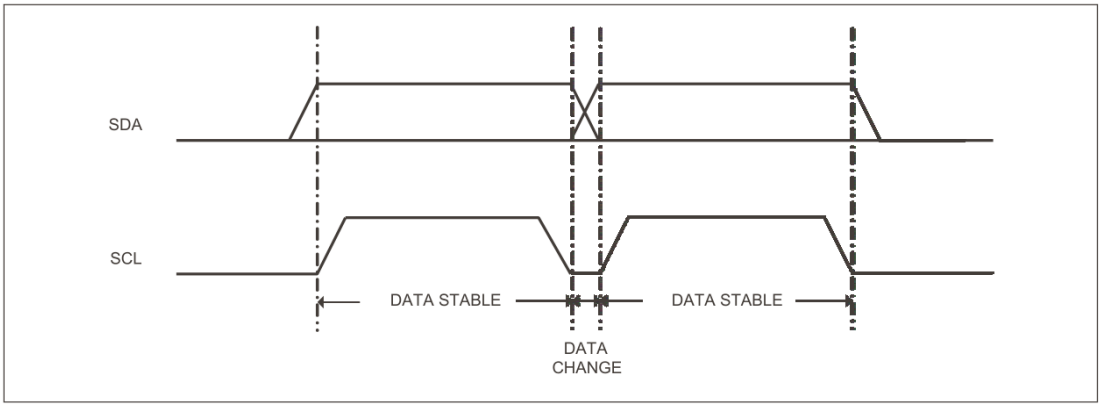


Figure 2: Start and Stop Definition

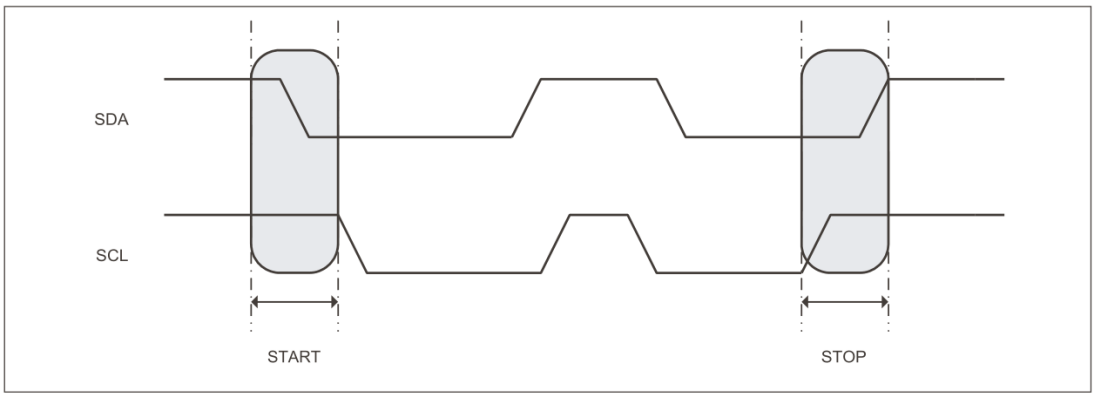
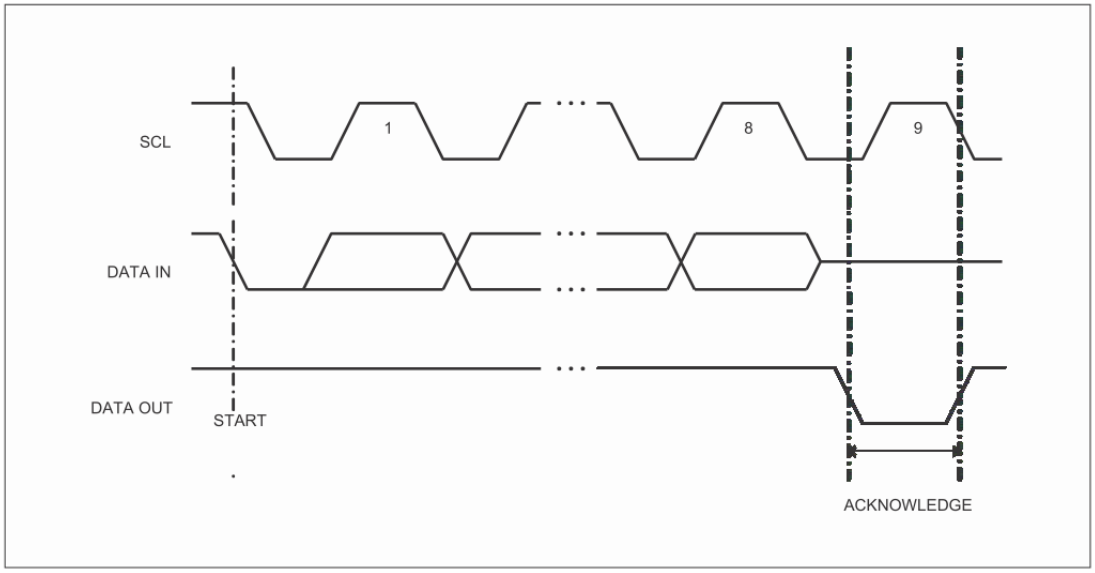


Figure 3: Output Acknowledge



Device Addressing

The 128K/256K/512K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see to Figure 4 on page 8)

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The 128K/256K/512K EEPROM uses A2, A1 and A0 device address bits to allow as much as eight devices on the same bus. These 3 bits must be compared to their corresponding hardwired input pins. The A2, A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

DATA SECURITY: The TX24C128/TX24C256/TX24C512 has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at VCC.

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 5 on page 8).

PAGE WRITE: The 128K/256K EEPROM is capable of an 64-byte page writes, and 512K device is capable of an 128-byte page writes.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 63 (128K/256K) or 127 (512K) more data words. The EEPROM will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 6 on page 8).

The data word address lower six (128K/256K) or seven (512K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 (128K/256K) or 128 (512K)

data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 7 on page 8).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 8 on page 9).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledgement. As long as the EEPROM receives an acknowledgement, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 9 on page 9).

Figure 4: Device Address

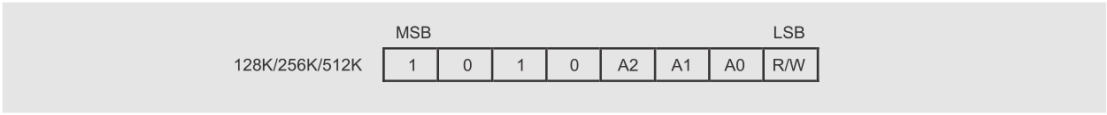


Figure 5: Byte Write

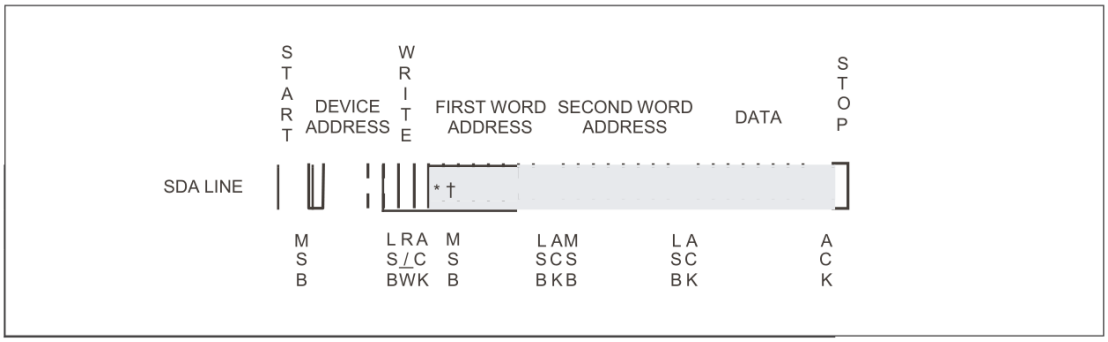
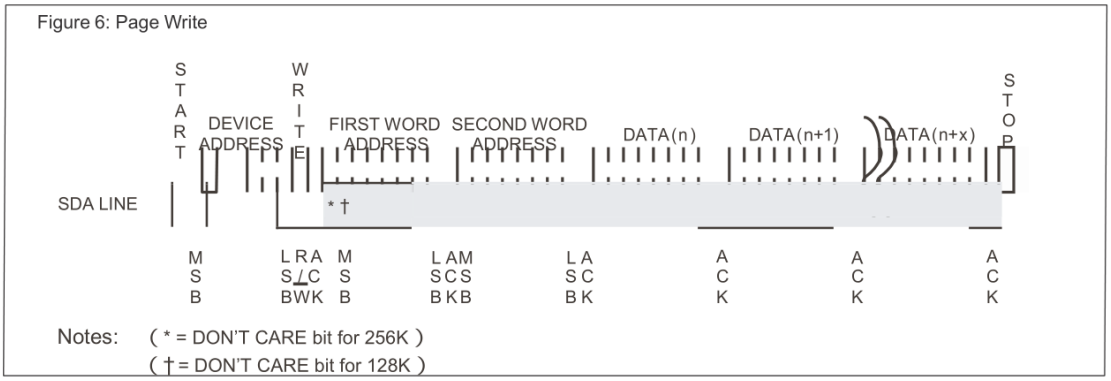


Figure 6: Page Write



Notes: (* = DON'T CARE bit for 256K)
(† = DON'T CARE bit for 128K)

Figure 7: Current Address Read

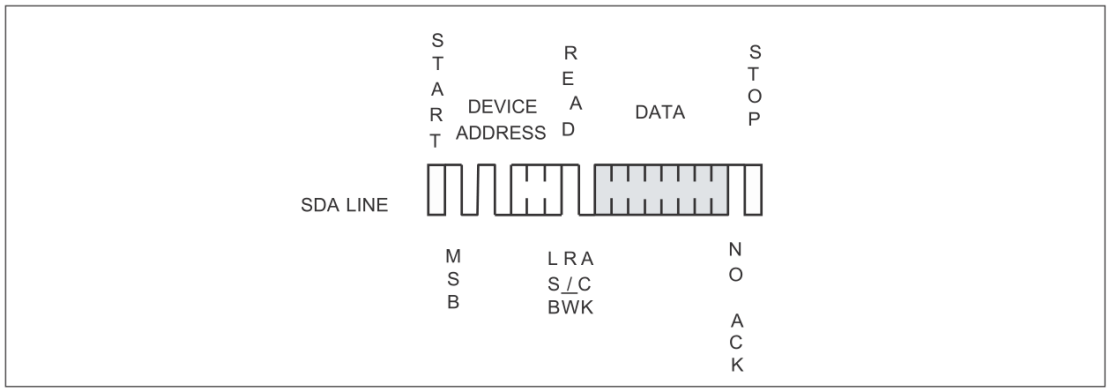


Figure 8: Random Read

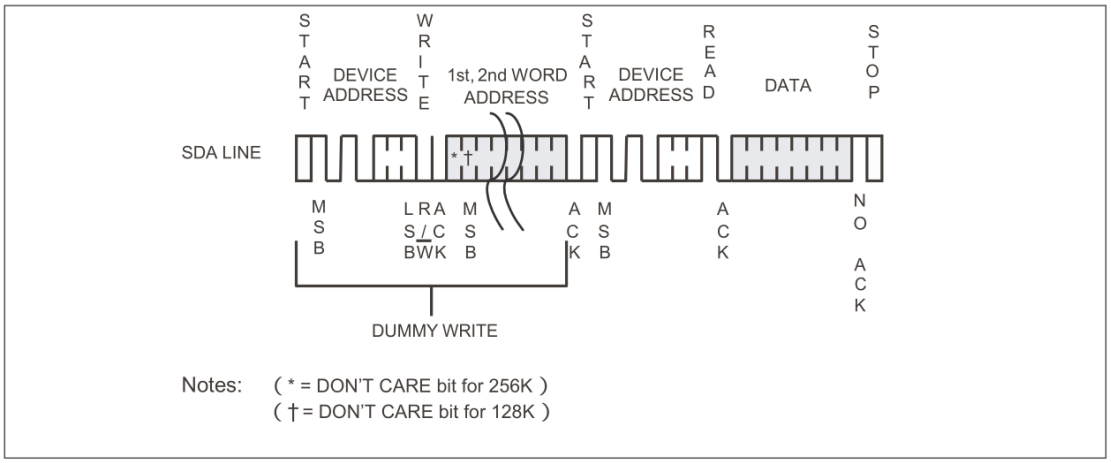
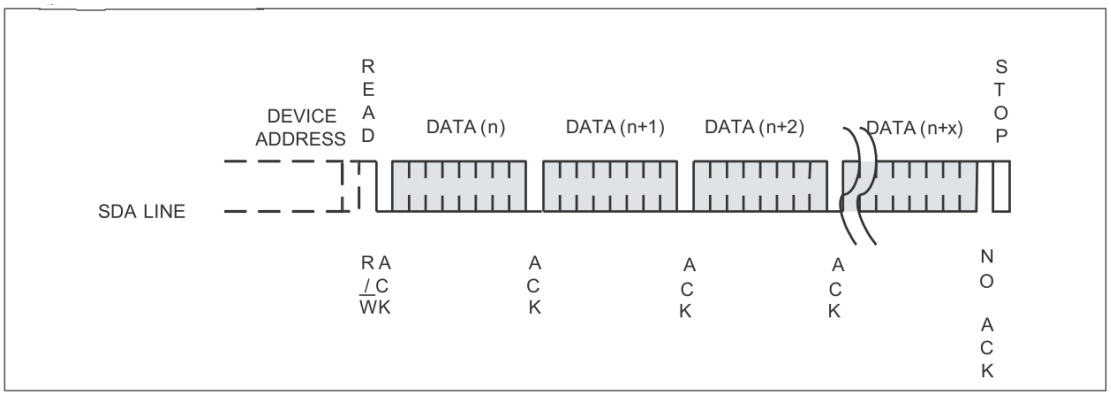


Figure 9: Sequential Read



Electrical Characteristics

Absolute Maximum Stress Ratings

DC Supply Voltage .....-0.3V to +6.5V

Input / Output Voltage..... GND-0.3V to VCC +0.3V

Operating Ambient Temperature .....-40℃ to +85℃

Storage Temperature..... -65℃ to +150℃

Comments

Stresses above those listed under "Absolute Maximum Ratings "may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Applicable over recommended operating range from: T_A= -40℃ to +85℃,VCC= +1.7V to +5.5V (unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage	V_{CC1}	1.7	-	5.5	V	
Supply Voltage	V_{CC2}	2.5	-	5.5	V	
Supply Voltage	V_{CC3}	2.7	-	5.5	V	
Supply Voltage	V_{CC4}	4.5	-	5.5	V	
Supply Current V_{CC}= 5.0V	I_{CC1}	-	0.4	1.0	mA	READ at 400 kHz
Supply Current V_{CC}= 5.0V	I_{CC2}	-	2.0	3.0	mA	WRITE at 400 kHz
Standby Current V_{CC}= 1.7V	I_{SB1}	-	0.6	1.0	uA	V_{IN}=V_{CC} or Vss
Standby Current V_{CC}= 2.5V	I_{SB2}	-	1.0	2.0	uA	V_{IN}=V_{CC} or Vss
Standby Current V_{CC}= 2.7V	I_{SB3}	-	1.0	2.0	uA	V_{IN}=V_{CC} or Vss
Standby Current VCC= 5.0V	I_{SB4}	-	2.0	5.0	uA	V_{IN}=V_{CC} or Vss
Input Leakage Current	I_{LI}	-	0.10	3.0	uA	V_{IN}=V_{CC} or Vss
Output Leakage Current	I_{LO}	-	0.05	3.0	uA	V_{OUT}=V_{CC} or Vss
Input Low Level	V_{IL1}	-0.3	-	V_{CC}x0.3	V	V_{CC}= 1.8V to 5.5V
Input High Level	V_{IH1}	V_{CC}x0.7	-	V_{CC}+0.3	V	V_{CC}= 1.8V to 5.5V
Input Low Level	V_{IL2}	-0.3	-	V_{CC}x0.2	V	V_{CC}= 1.7V
Input High Level	V_{IH2}	V_{CC}x0.7	-	V_{CC}+0.3	V	V_{CC}= 1.7V
Output Low Level V_{CC}=5.0V	V_{OL3}	-	-	0.4	V	I_{OL}= 3.0 mA
Output Low Level V_{CC}=3.0V	V_{OL2}	-	-	0.4	V	I_{OL}= 2.1 mA
Output Low Level V_{CC}=1.7V	V_{OL1}	-	-	0.2	V	I_{OL}= 0.15 mA

Pin Capacitance

Applicable over recommended operating range from T_A=25℃, f=1.0MHz,VCC=+1.7V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input /Output Capacitance (SDA)	$C_{I/O}$	-	-	8	pF	$V_{I/O}$= 0V
Input Capacitance (A0, A1, A2,SCL)	C_{IN}	-	-	6	pF	V_{IN}= 0V

AC Electrical Characteristics

Applicable over recommended operating range from T_A= -40℃ to +85℃,VCC= +1.7V to +5.5V,C_L=1TTL Gate and 100 pF (unless otherwise noted)

Parameter	Symbol	1.7v≤Vcc < 2.5v			2.5v≤Vcc≤5.5v			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency, SCL	F_{SCL}	-	-	400	-	-	1000	kHz
Clock Pulse Width Low	T_{LOW}	1.2	-	-	0.6	-	-	us
Clock Pulse Width High	T_{HIGH}	0.6	-	-	0.4	-	-	us
Noise Suppression Time	T_I	-	-	50	-	-	50	ns
Clock Low to Data Out Valid	T_{AA}	0.1	-	0.9	0.05	-	0.9	us
Time the bus must be free before a new transmission can start	T_{BUF}	1.2	-	-	0.5	-	-	us
Start Hold Time	$T_{HD.STA}$	0.6	-	-	0.25	-	-	us
Start Setup Time	$T_{SU.STA}$	0.6	-	-	0.25	-	-	us
Data In Hold Time	$T_{HD.DAT}$	0	-	-	0	-	-	us
Data In Setup Time	$T_{SU.DAT}$	100	-	-	100	-	-	ns
Inputs Rise Time(1)	T_R	-	-	0.3	-	-	0.3	us
Inputs Fall Time(1)	T_F	-	-	300	-	-	300	ns
Stop Setup Time	$T_{SU.STO}$	0.6	-	-	0.25	-	-	us
Data Out Hold Time	T_{DH}	50	-	-	50	-	-	ns
Write Cycle Time	T_{WR}	-	3.3	5	-	3.3	5	ms
5.0V,25℃, Byte Mode	Endurance	1M	-	-	-	-	-	Write Cycles

Note: 1.This parameter is characterized and is not 100% tested.

2.AC measurement conditions: R_L(connects to V_{CC}): 1.3kΩ（2.5V，5V），10kΩ（1.7V）

Input pulse voltages: 0.3 V_{CC} to 0.7V_{CC}

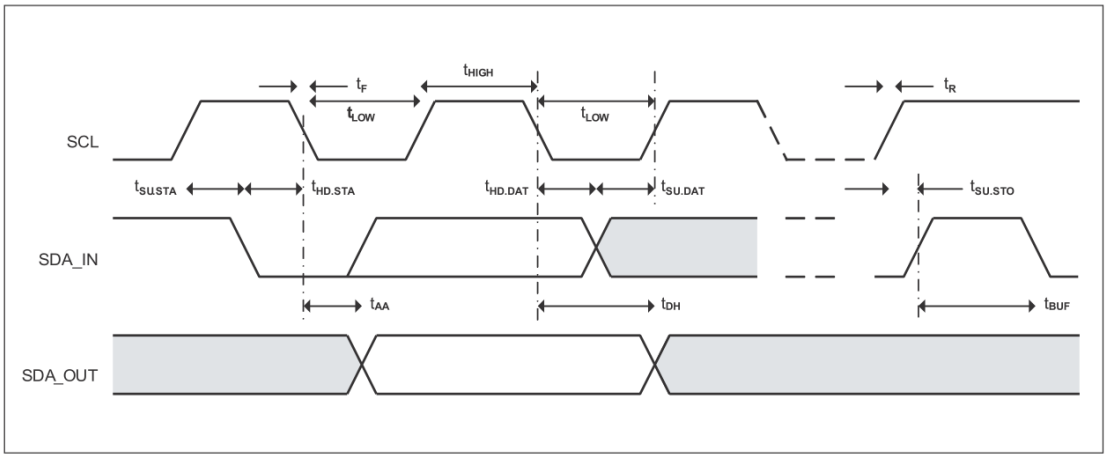
Input rise and fall time: ≤50ns

Input and output timing reference voltages: 0.5 V_{CC}

The value of R_L should be concerned according to the actual loading on the user's system.

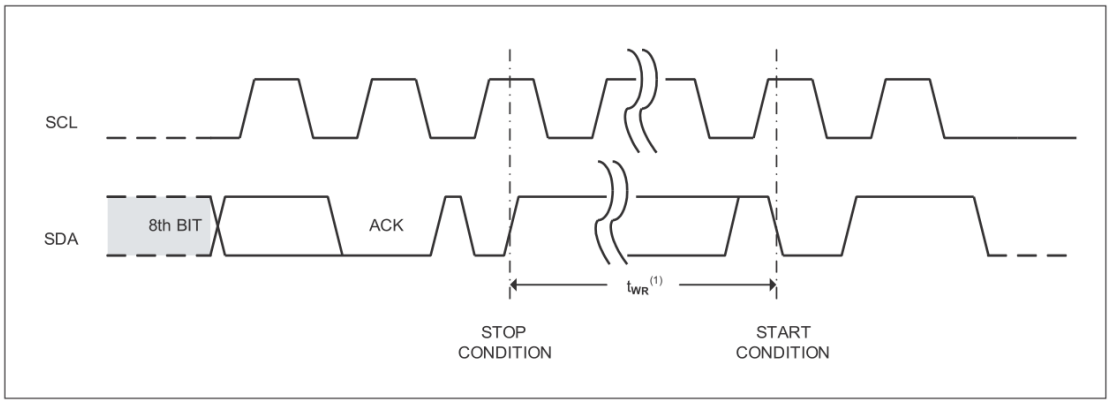
Bus Timing

Figure 10: SCL: Serial Clock, SDA: Serial Data I/O



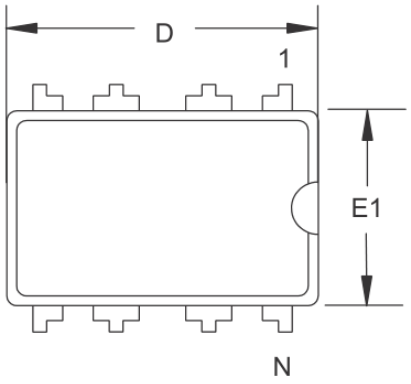
Write Cycle Timing

Figure 11: SCL: Serial Clock, SDA: Serial Data I/O

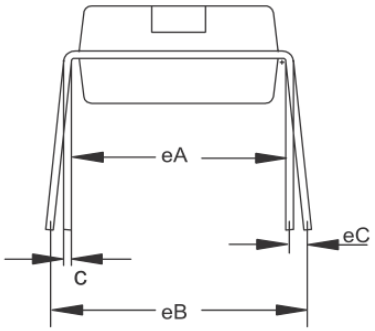


Note: 1. Write cycle time TWR is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

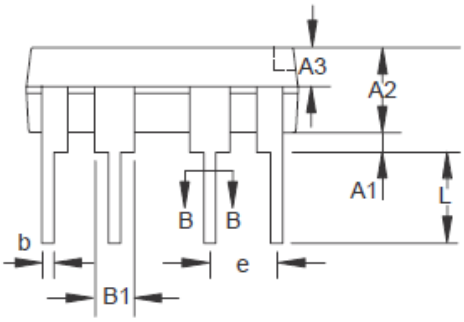
8-lead DIP package diagram



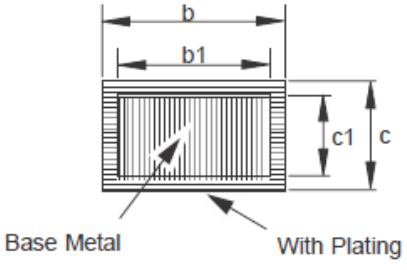
Top View



End View



Side View

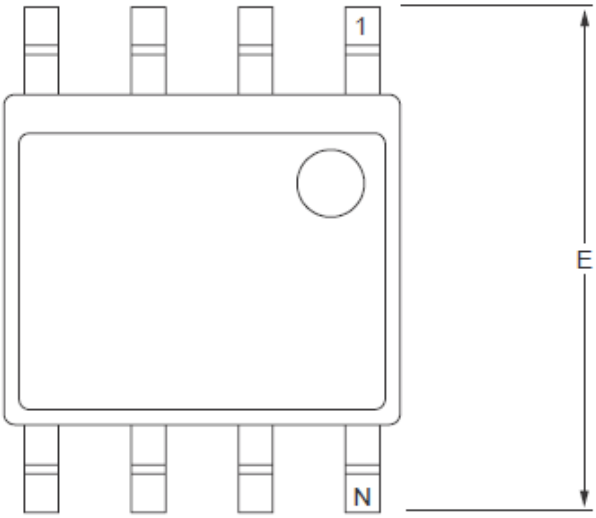


Section B-B

COMMON DIMENSIONS
(Unit of Measure = mm)

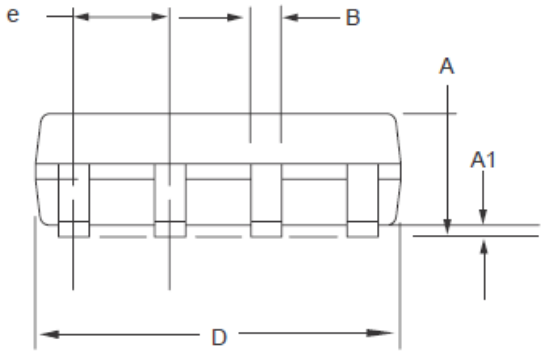
SYMBOL	MIN	MAX
A	3.60	4.00
A1	0.51	-
A2	3.10	3.50
A3	1.50	1.70
b	0.44	0.53
b1	0.43	0.48
B	1.52 BSC	
c	0.25	0.31
c1	0.24	0.26
D	9.05	9.45
E1	6.15	6.55
e	2.54 BSC	
eA	7.62 BSC	
eB	7.62	9.50
eC	0	0.94
L	3.00	-

8-lead SOP package diagram



Top View

End View

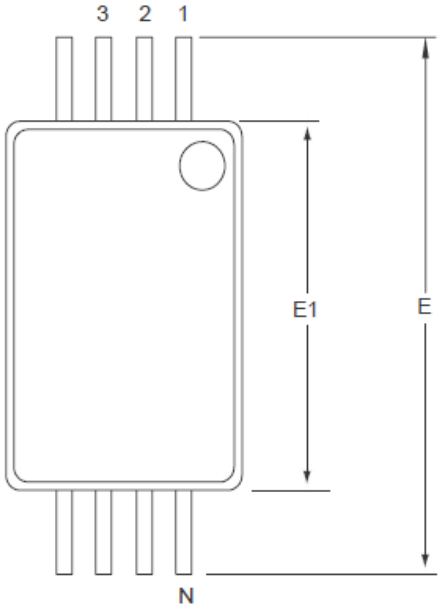


Side View

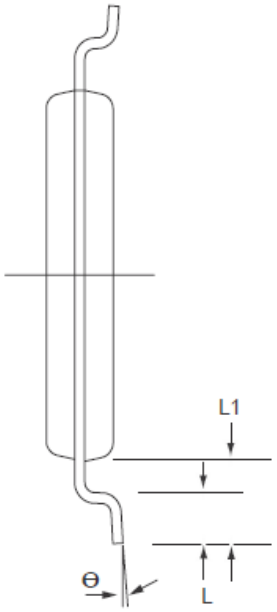
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.31	0.51
C	0.17	0.25
D	4.70	5.10
E1	3.80	4.00
E	5.79	6.20
e	1.27 BSC	
L	0.40	1.27
θ	0°	8°

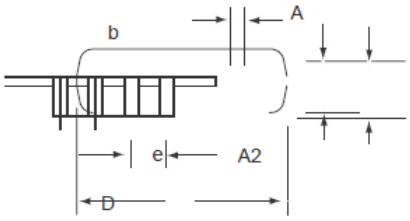
8-lead TSSOP package diagram



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	MAX
D	2.80	3.20
E	6.20	6.90
E1	4.20	4.60
A	–	1.20
A2	0.80	1.15
b	0.19	0.30
e	0.65 BSC	
L	0.45	0.75
L1	1.00 BSC	
θ	0^0	8^0