



# TX6212B Series

## High Speed Low Noise LDO

### Features

- Low power consumption:10uA (Typ.)
- Low voltage drop:  
0.11V@100mA@VOUT=2.8V(Typ.)
- Standby Mode: 0.1uA
- Low temperature coefficient
- Good line Regulation:0.05%/V
- High Ripple Rejection: 75dB@100Hz(Typ.)
- High input voltage (up to 6.5V)
- Output voltage accuracy: tolerance  $\pm 2\%$
- SOT23-5, SOT23-3, SOT23 and DFN1\*1 packages

### Applications

- Battery-powered equipment
- Communication equipment
- Mobile phones
- Portable games
- Cameras, Video cameras
- Reference voltage sources

### General Description

The TX6212B series are highly accurate, low noise, CMOS LDO Voltage Regulators. Offering low output noise, high ripple rejection ratio, low dropout and very fast turn-on times, the TX6212B series is ideal for today's cutting edge mobile phone. Internally the TX6212B includes a reference voltage source, error amplifiers, driver transistors, current limiters and phase compensators.

The TX6212B's output voltage is set by current trimming. Voltages are selectable in 100mV steps within a range of 0.9V to 5.0V.

When the CE input pin is low, the fast discharge

channel can pass, a built-in pull-down resistor pulls the output voltage low. Fast discharge function.

The TX6212B series is also fully compatible with low ESR ceramic capacitors, reducing cost and improving output stability. This high level of output stability is maintained even during frequent load fluctuations, due to the excellent transient response performance and high PSRR achieved across a broad range of frequencies. The CE function allows the output of regulator to be turned off, resulting in greatly reduced power consumption.

### Order Information

#### TX6212B-①②③④

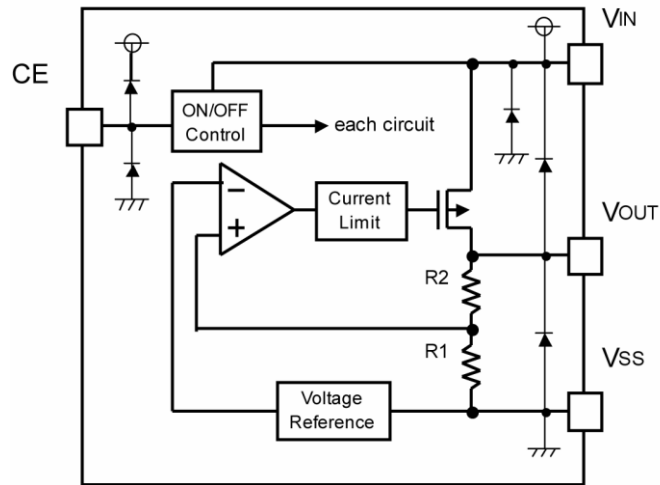
Designator	Symbol	Description
①②	Integer	Output Voltage
③	M5	Package: SOT23-5
	M	Package: SOT23-3
	N	Package: SOT23
	FC	Package: DFN1*1
④	R	RoHS / Pb Free
	G	Halogen Free

Note:"①②" stands for output voltages. Other voltages can be specially customized



# TX6212B Series High Speed Low Noise LDO

## Block Diagram



## Package and Pin assignment

SOT23-3 and SOT23 (Top View)

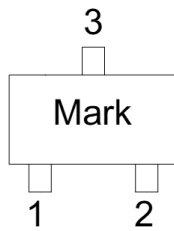


Table1: TX6212B-XXMR series (SOT23-3 and SOT23 PKG)

PIN NO.	PIN NAME	FUNCTION
1	GND	GND pin
2	VOUT	Output voltage pin
3	VIN	Input voltage pin

SOT23-5 (Top View)

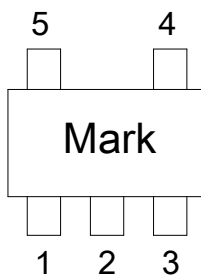


Table2: TX6212B-XXM5R series (SOT23-5 PKG)

PIN NO	PIN NAME	FUNCTION
1	VIN	Input
2	GND	Ground
3	EN	Enable(Active high, not floating)
4	NC	Not connected
5	VOUT	Output

DFN1\*1-4L

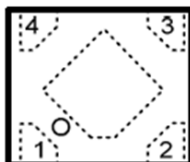


Table3: TX6212B-XXFCR series (DFN1\*1-4PKG)

PIN NO	PIN NAME	FUNCTION
1	VOUT	Output
2	GND	Ground
3	EN	Enable(Active high, not floating)
4	VIN	Input



## TX6212B Series

### High Speed Low Noise LDO

#### Marking Rule

MARKING	
VOLTAGE(V)	Package
	SOT23-5、SOT23-3、SOT23、DFN1*1
1.2	LVBX
1.5	LVEX
1.8	LVKX
2.5	LVFX
2.8	LVXX
3.0	LVZX
3.3	LV2X

#### Absolute Maximum Ratings

Supply Voltage .....-0.3V to 8V

Storage Temperature .....-50℃ to 125℃

Operating Temperature .....-40℃ to 85℃

Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

#### Thermal Information

Symbol	Parameter	Package	Max.	Unit
$\theta_{JA}$	Thermal Resistance (Junction to Ambient) (Assume no ambient airflow, no heat sink)	SOT23-5	260	℃/W
		SOT23-3	260	
		SOT23	280	
		DFN1*1	250	
$P_D$	Power Dissipation	SOT23-5	0.4	W
		SOT23-3	0.4	
		SOT23	0.2	
		DFN1*1	0.4	

Note:  $P_D$  is measured at  $T_a = 25^\circ\text{C}$



# TX6212B Series

## High Speed Low Noise LDO

### Electrical Characteristics

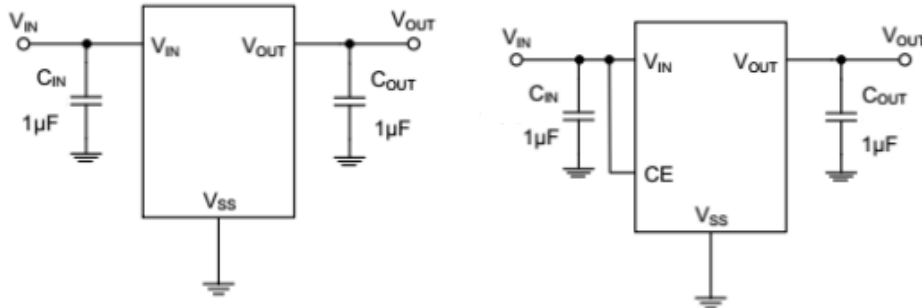
TX6212B series

(Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	Vout≤2.5V	Vin=Vout+1V 1.0mA≤Iout≤100mA	Vout -0.05		Vout +0.05	V
	2.5V≤Vout≤5V	Vin=Vout+1V 1.0mA≤Iout≤300mA	Vout×0.98	--	Vout×1.02	V
Output Current*1	Iout	Vin-Vout=1V	--	300	--	mA
Line Regulation	$\Delta V_{out} / (\Delta V_{in} \cdot V_{out})$	4.3V≤Vin≤8V Iout=10mA	--	0.05	0.2	%/V
Load Regulation	$\Delta V_{out}$	Vin= 4.3V 1.0mA≤Iout≤100mA	--	15	40	mV
Dropout Voltage	V <sub>DROP</sub>	Iout=100mA	--	0.11	--	V
Output voltage Temperature Coefficiency	$\Delta V_{out} / (Ta \cdot V_{out})$	Iout=30mA 0°C≤Ta≤70°C	--	±100	--	Ppm/°C
Supply Current	I <sub>ss</sub>	--	--	10	15	uA
Input Voltage	Vin	--	--	--	6.5	V
EN logic high voltage	V <sub>ENH</sub>	VIN=5.0V	1.5	--	--	V
EN logic low voltage	V <sub>ENL</sub>	VIN=5.0V	--	--	0.4	V
PSRR	PSRR	F=100Hz, Vin= (VOUT+1) dc+1Vpp	--	75	--	dB
		F=1000Hz, Vin= (VOUT+1) dc+1Vpp	--	65	--	dB



### Typical Application Circuit



### Operational Explanation

#### <Low ESR Capacitors>

With the TX6212B series, a stable output voltage is achievable even if used with low ESR capacitors as a phase compensation circuit is built-in. In order to ensure the effectiveness of the phase compensation, we suggest that an output capacitor ( $C_L$ ) is connected as close as possible to the output pin ( $V_{OUT}$ ) and the  $V_{SS}$  pin. Please use an output capacitor with a capacitance value of at least 10 $\mu$ F. Also, please connect an input capacitor ( $C_{IN}$ ) of 10 $\mu$ F between the  $V_{IN}$  pin and the  $V_{SS}$  pin in order to ensure a stable power input. Stable phase compensation may not be ensured if the capacitor runs out capacitance when depending on bias and temperature. In case the capacitor depends on the bias and temperature, please make sure the capacitor can ensure the actual capacitance.

#### <CE Pin>

The IC's internal circuitry can be shutdown by the signal from the CE pin with the TX6212B series. In shutdown mode, output at the  $V_{OUT}$  pin will be pulled down to the  $V_{SS}$ . Although the CE pin is equal to an inverter input with CMOS hysteresis, with either the pull-up or pull-down options, the CE pin input current will increase when the IC is in operation. If you want add resistor before the CE pin, the resistor must be under 10K. We suggest that you use this IC with either a  $V_{IN}$  voltage or a  $V_{SS}$  voltage input at the CE pin. If this IC is used with the correct specifications for the CE pin, the operational logic is fixed and the IC will operate normally. However, supply current may increase as a result of through current in the IC's internal circuitry.

### Notes on Use

1. Please use this IC within the stated absolute maximum ratings. The IC is liable to malfunction should the ratings be exceeded.
2. Where wiring impedance is high, operations may become unstable due to noise and/or phase lag depending on output current. Please keep the resistance low between  $V_{IN}$  and  $V_{SS}$  wiring in particular.
3. Please wire the input capacitor ( $C_{IN}$ ) and the output capacitor ( $C_L$ ) as close to the IC as possible.

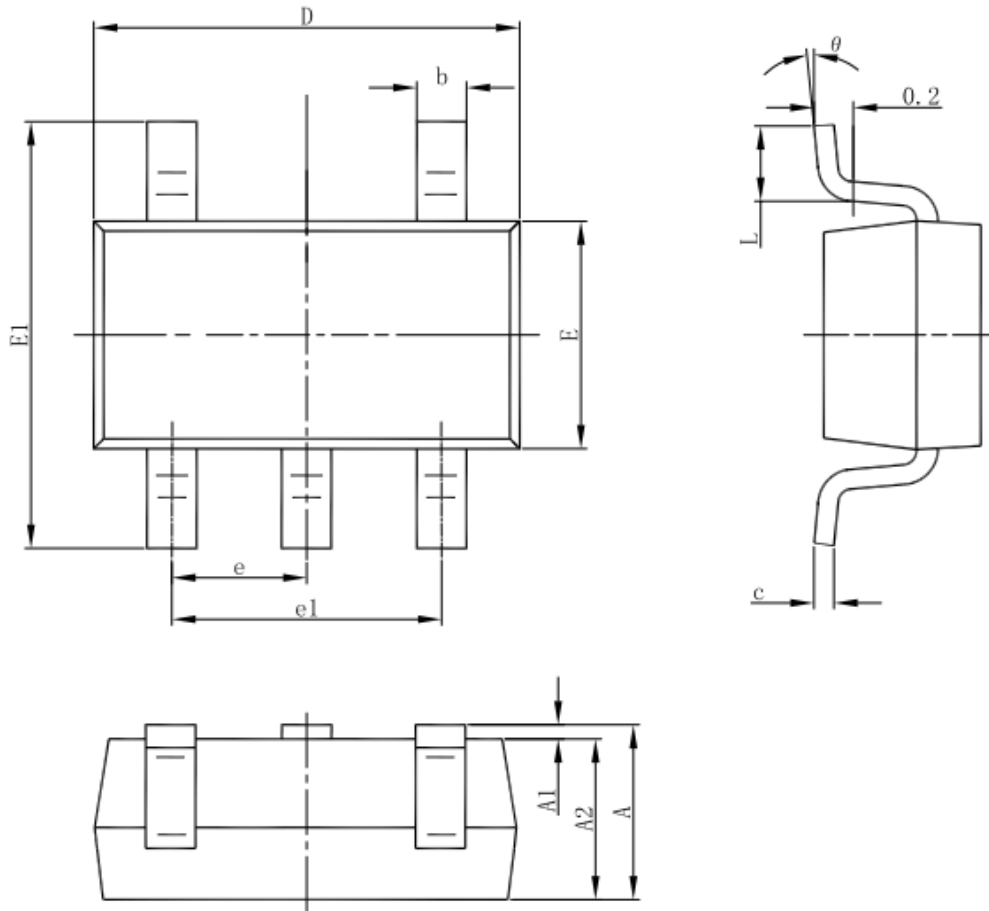


# TX6212B Series

## High Speed Low Noise LDO

### Packaging Information

#### SOT23-5 Outline Dimensions

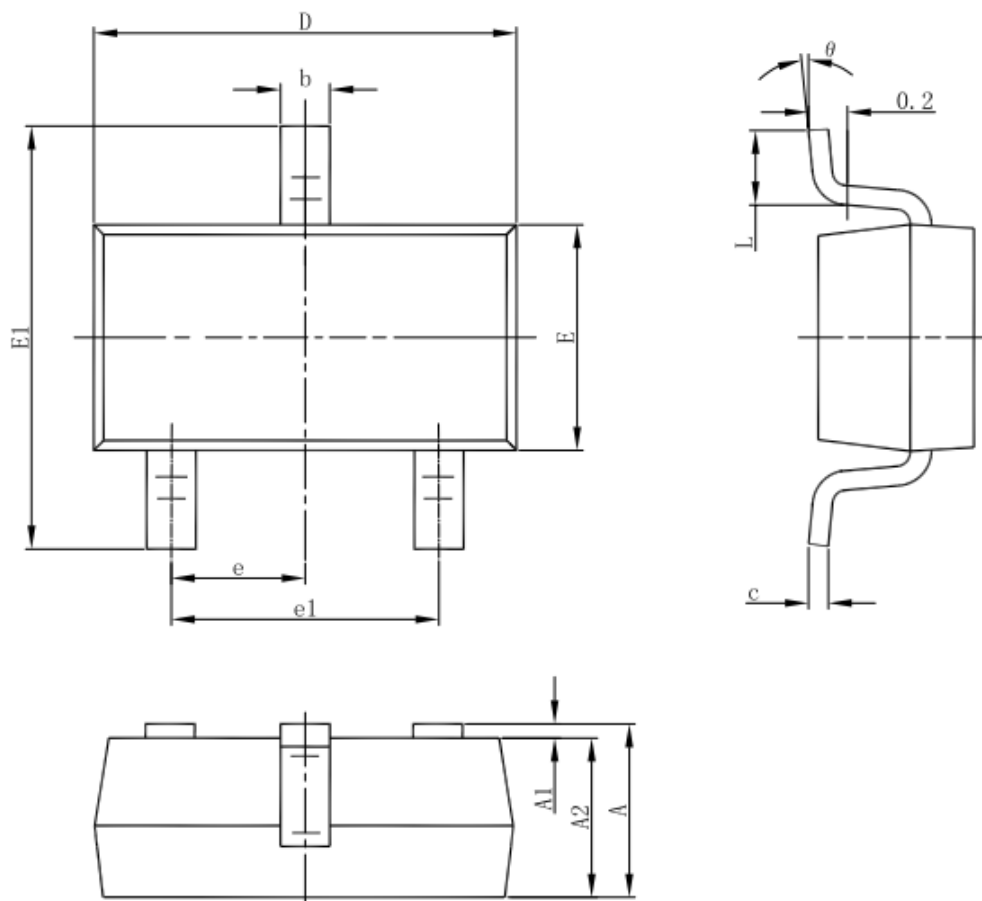


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°



## TX6212B Series High Speed Low Noise LDO

### 3-pin SOT23-3 Outline Dimensions



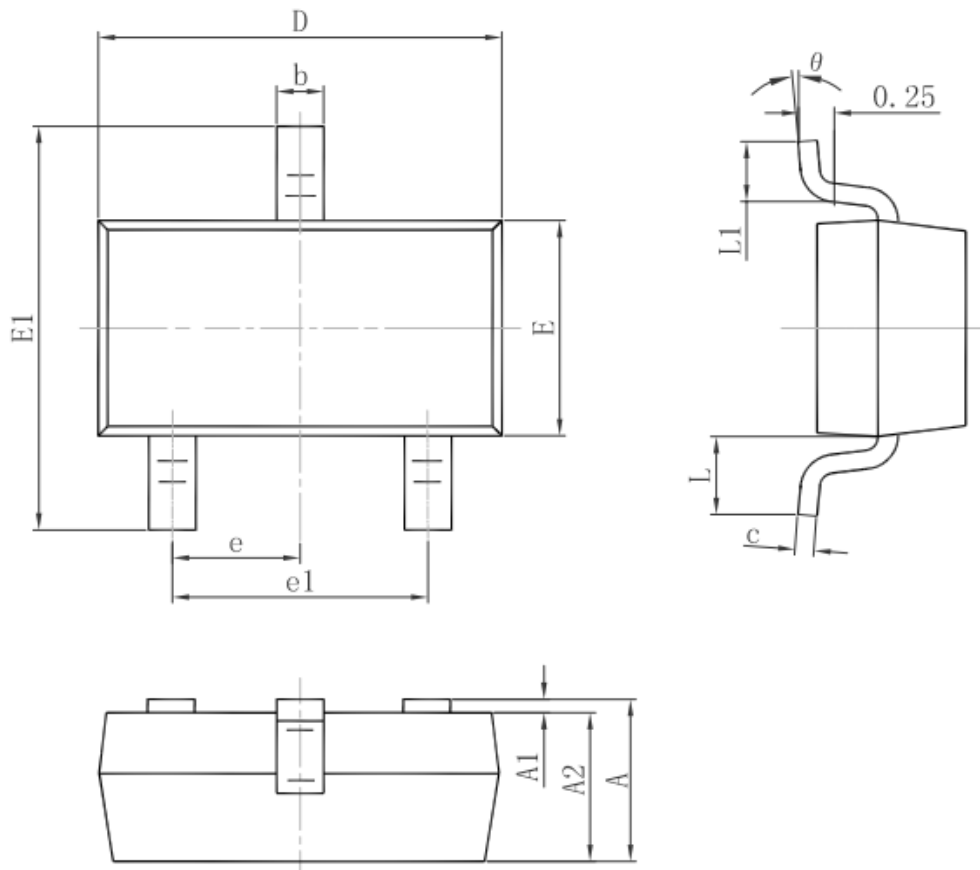
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°



<http://www.txsemi.com>

## TX6212B Series High Speed Low Noise LDO

### 3-pin SOT23 Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
$\theta$	0°	8°	0°	8°



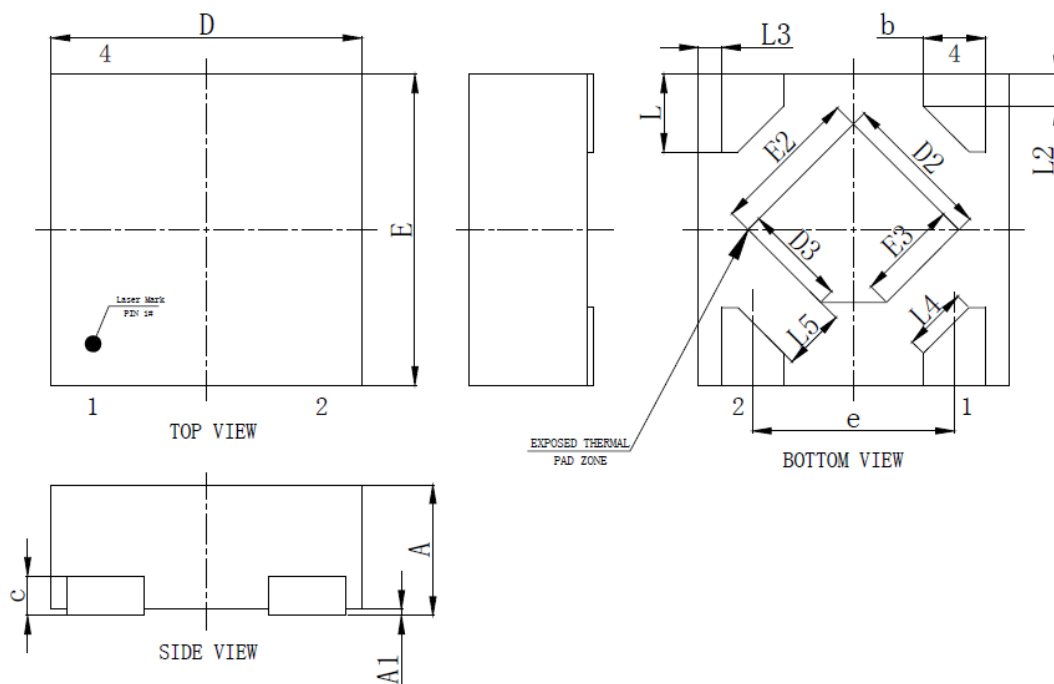


<http://www.txsemi.com>

# TX6212B Series

## High Speed Low Noise LDO

### DFN1\*1-4 Outline Dimensions



SYMBOL	MILLIMETER		
	MIN	MID	MAX
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	0.127REF		
D	0.95	1.00	1.05
D2	0.38	0.48	0.58
D3	0.23	0.33	0.43
e	0.65BSC		
E	0.95	1.00	1.05
E2	0.38	0.48	0.58
E3	0.23	0.33	0.43
L	0.20	0.25	0.30
L2	0.103REF		
L3	0.075REF		
L4	0.208REF		
L5	0.200REF		



<http://www.txsemi.com>

## ***TX6212B Series***

### ***High Speed Low Noise LDO***

---

© Shanghai TX Semiconductor Sci.-Tech. Co., Ltd.

TX cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a TX product. No circuit patent license, copyrights or other intellectual property rights are implied. TX reserves the right to make changes to their products or specifications without notice. Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete.