



# TX61C series

## Low Power Voltage Detector

### Features

- Low power consumption
- Low temperature coefficient
- Built-in hysteresis characteristic
- High input voltage (up to 8V)
- Output voltage accuracy:
  - $\pm 2\% @ V_{DET} \geq 2.5V$
  - $\pm 50mV @ V_{DET} < 2.5V$
- SOT23, SOT23-3 and DFN1\*1-4L package

### Applications

- Battery checkers
- Level selectors
- Power failure detectors
- Microcomputer reset
- Battery memory backup
- Non-volatile RAM signal storage protectors

### General Description

The TX61C series devices are a set of three terminal low power voltage detectors implemented in CMOS technology. Each voltage detector in the series detects a particular fixed voltage ranging from 0.9V to 5.0V. The voltage detectors consist of a high-precision and low power consumption standard voltage source as well as a comparator,

hysteresis circuit, and an output driver (CMOS inverter or NMOS open drain). CMOS technology ensures low power consumption.

Although designed primarily as fixed voltage detectors, these devices can be used with external components to detect user specified threshold voltages.

### Selection Table

Part No.	Det. Voltage	Hys. Width	Output	Tolerance	Package
TX61CC0902MR	0.9V	5%	CMOS	$\pm 50mV$	SOT23 SOT23-3 DFN1*1
TX61CN0902MR	0.9V	5%	NMOS	$\pm 50mV$	
TX61CC1002MR	1.0V	5%	CMOS	$\pm 50mV$	
TX61CN1002MR	1.0V	5%	NMOS	$\pm 50mV$	
...	...	...	...	...	
TX61CC2402MR	2.4V	5%	CMOS	$\pm 50mV$	
TX61CN2402MR	2.4V	5%	NMOS	$\pm 50mV$	
TX61CC2502MR	2.5V	5%	CMOS	$\pm 2\%$	
TX61CN2502MR	2.5V	5%	NMOS	$\pm 2\%$	
...	...	...	...	$\pm 2\%$	
TX61CC5002MR	5.0V	5%	CMOS	$\pm 2\%$	
TX61CN5002MR	5.0V	5%	NMOS	$\pm 2\%$	



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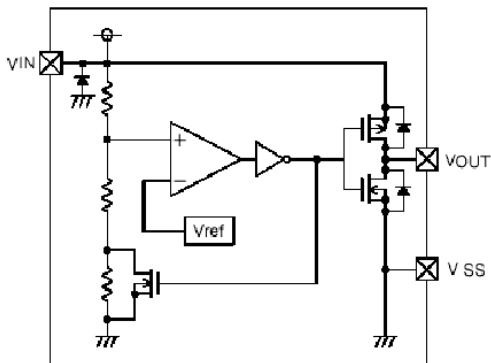
## Order Information

TX61C①②③④⑤⑥⑦

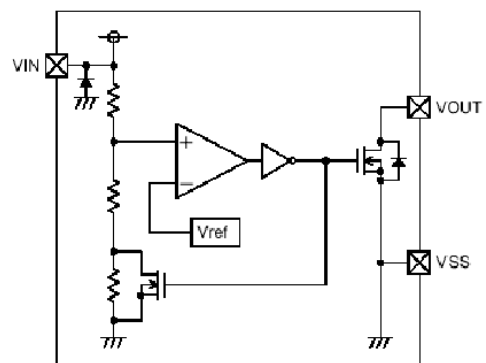
Designator	Symbol	Description
①	C	CMOS output
	N	NMOS output
②③	VOUT	Output Voltage(0.9~5.0V)
④⑤	02	Standard
⑥	N	Package: SOT23
	M	Package: SOT23-3
	FC	Package: DFN1*1-4L
⑦	R	RoHS / Pb Free
	G	Halogen Free

## Block Diagram

(1) CMOS Output



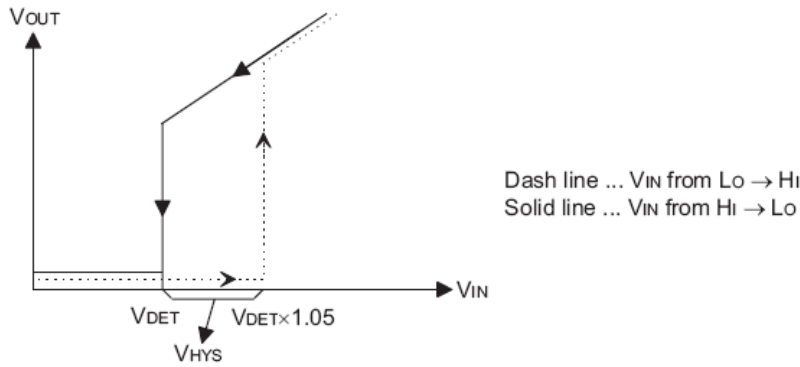
(2) N-ch Open Drain Output





**Output Table & Curve**

$V_{DD}$	$V_{DD} > V_{DET}(+)$	$V_{DD} \leq V_{DET}(-)$
$V_{OUT}$	Hi-Z	$V_{SS}$



**Pin Assignment**

SOT23 and SOT23-3

(Top View)

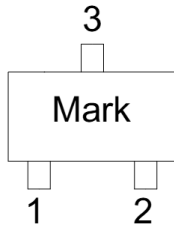


Table1: TX61C series (SOT23 and SOT23-3 PKG)

PIN NO.	PIN NAME	FUNCTION
1	VOUT	Output voltage pin
2	GND	GND pin
3	VIN	Input voltage pin

DFN1\*1-4L

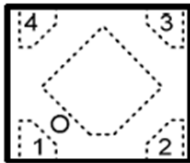


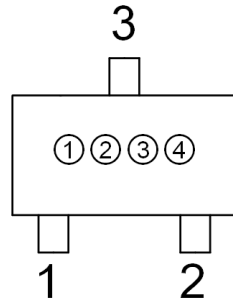
Table2: TX61C series (DFN1\*1-4PKG)

PIN NO	PIN NAME	FUNCTION
1	VOUT	Output
2	GND	Ground
3	NC	No connect
4	VIN	Input

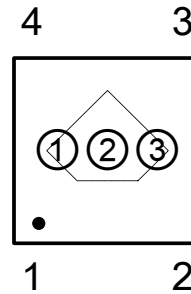


### Marking Rule

SOT23 and SOT23-3



DFN1\*1-4L



① Represents integer of detect voltage

CMOS Output

MARK	CONFIGURATION	VOLTAGE (V)
A	CMOS	0.x
B	CMOS	1.x
C	CMOS	2.x
D	CMOS	3.x
E	CMOS	4.x
F	CMOS	5.x
H	CMOS	6.x

N-Channel Open Drain Output

MARK	CONFIGURATION	VOLTAGE (V)
K	N-ch	0.x
L	N-ch	1.x
M	N-ch	2.x
N	N-ch	3.x
P	N-ch	4.x
R	N-ch	5.x
S	N-ch	6.x

② Represents decimal number of detect voltage

MARK	VOLTAGE (V)	MARK	VOLTAGE (V)
0	x.0	5	x.5
1	x.1	6	x.6
2	x.2	7	x.7
3	x.3	8	x.8
4	x.4	9	x.9

③ ④ Represents production lot number



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### Absolute Maximum Ratings

Supply Voltage .....-0.3V to 8.5V      Storage Temperature .....-50°C to 125°C  
 Operating Temperature .....-40°C to 85°C

Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

### Thermal Information

Symbol	Parameter	Package	Max.	Unit
$\theta_{JA}$	Thermal Resistance (Junction to Ambient) (Assume no ambient airflow, no heat sink)	SOT23-3	500	°C/W
$P_D$	Power Dissipation	SOT23-3	0.20	W

Note:  $P_D$  is measured at  $T_a = 25^\circ\text{C}$

### Electrical Characteristics

$V_{DF} = 0.8\text{V} \sim 5.0\text{V}$

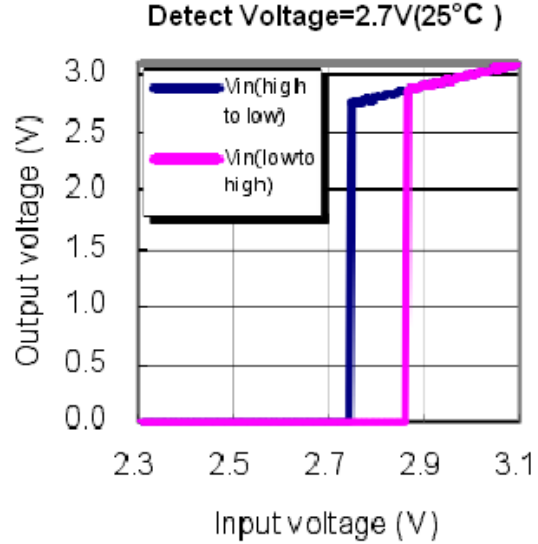
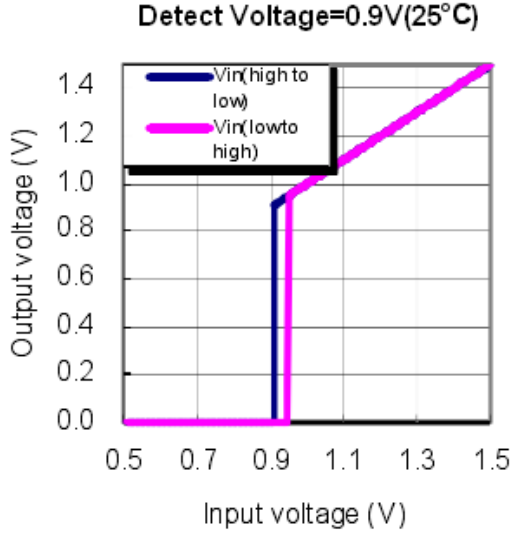
$T_a = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{DET}$	Detection Voltage	$V_{DF} = 0.9\text{V} \sim 2.4\text{V}$	$V_{DET} - 0.05$	$V_{DET}$	$V_{DET} + 0.05$	V
		$V_{DF} = 2.5\text{V} \sim 5.0\text{V}$	$V_{DET} * 0.98$	$V_{DET}$	$V_{DET} * 1.02$	V
$V_{HYS}$	Hysteresis Width	-	$0.02 * V_{DET}$	$0.05 * V_{DET}$	$0.10 * V_{DET}$	V
$I_{DD}$	Operating Current	$V_{in} = 1.5\text{V}$	-	0.7	2.3	$\mu\text{A}$
		$V_{in} = 2.0\text{V}$	-	0.8	2.7	
		$V_{in} = 3.0\text{V}$	-	0.9	3.0	
		$V_{in} = 4.0\text{V}$	-	1.0	3.2	
		$V_{in} = 5.0\text{V}$	-	1.1	3.6	
$V_{DD}$	Operating Voltage	-	0.7	-	8.5	V
Tdelay	$V_{in}$ from low to high	$V_{DET} = 2.9\text{V}$	-	55	-	us
Tperiod	$V_{in}$ from high to low	$V_{DET} = 2.9\text{V}$	-	0.5	-	us
$I_{OL}$	Output Sink Current	2V $V_{OUT} = 0.2\text{V}$	0.5	1	-	mA
$\frac{\Delta V_{DET}}{V_{DF} \Delta T_a}$	Temperature Coefficient	-	-25°C < $T_a$ >125°C	-	$\pm 100$	ppm/°C

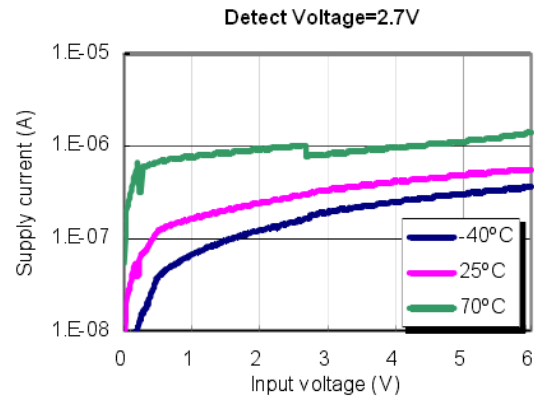
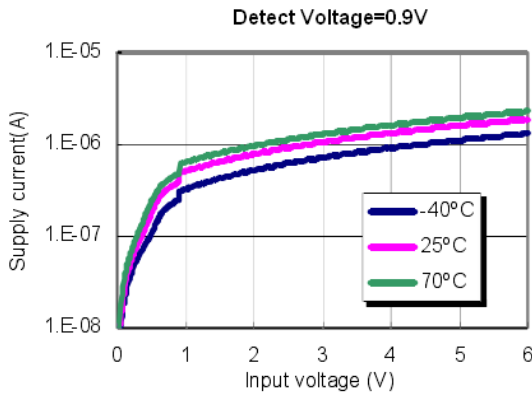


Typical Performance Characteristics

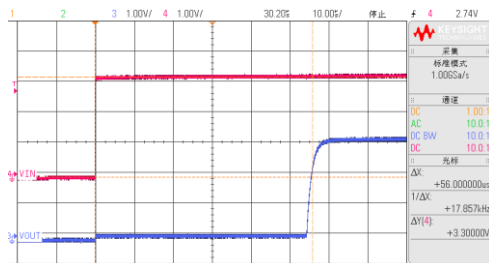
(1) Output Voltage vs Input voltage



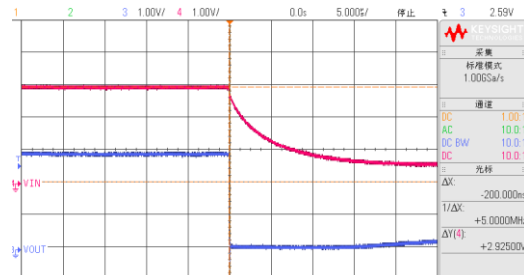
(2) Supply Current vs. Input Voltage



(3) Vin from 0 to 3.3V delay  
Tdelay=56us



(4) Vin from 3.3V to 0V delay  
Tperiod=200ns



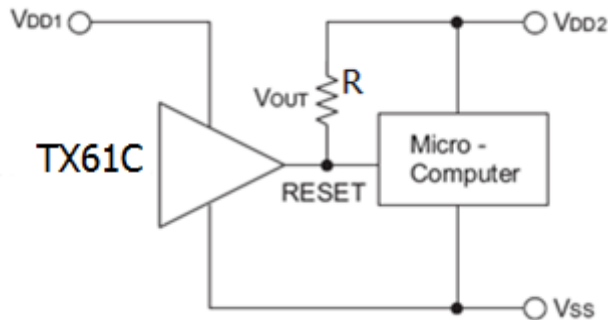


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## Microcomputer Reset Circuit

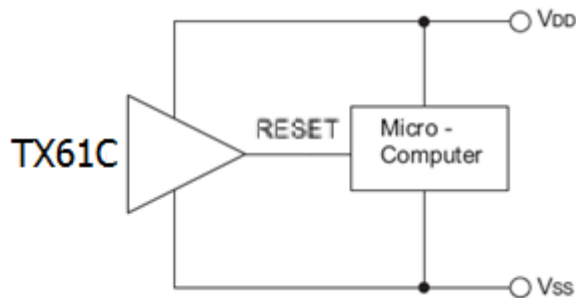
Normally a reset circuit is required to protect the microcomputer system from malfunctions due to power line interruptions. The following examples show how different output configurations perform a reset function in various systems.

NMOS open drain output application for separate power supply



R=47K

CMOS output application



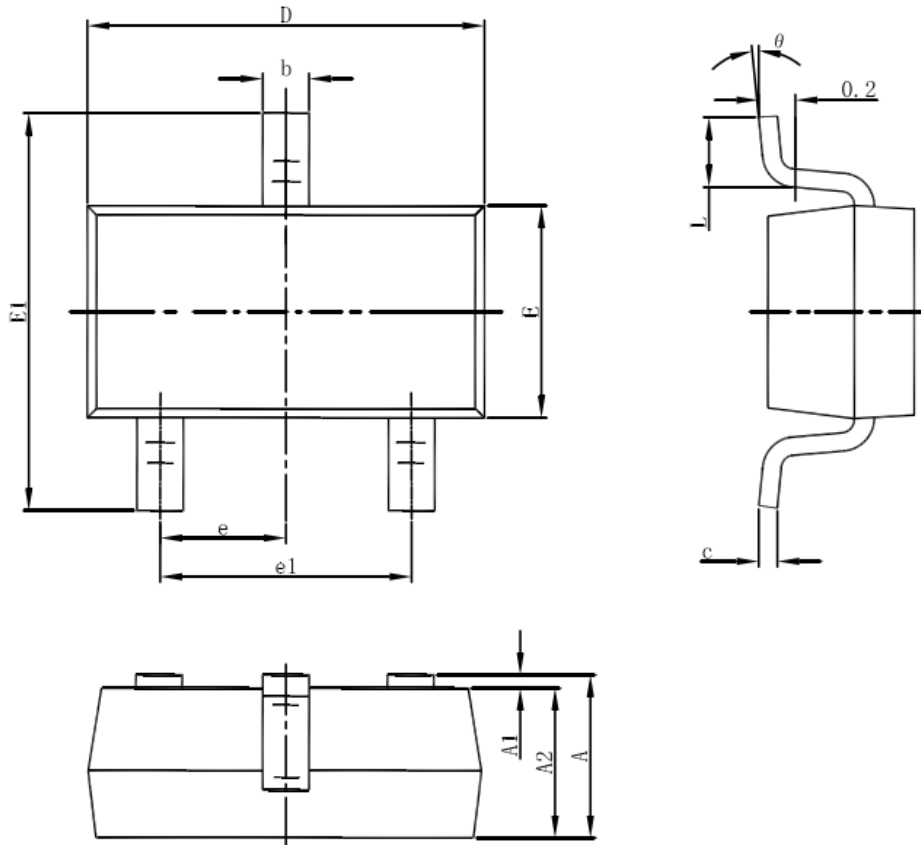


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# TX61C series Low Power Voltage Detector

## Package Information

### 3-pin SOT23-3 Outline Dimensions







Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
theta	0°	8°	0°	8°





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封装形式	SOT
载带	W: 8mm
盖带	W: 5.3mm
卷盘	7寸*8.4mm; 蓝盘
	 ↑ 正面
	 ↑ 反面
包装袋	235*255mm 屏蔽袋
内盒	205*205*210mm
	
外箱	430*430*230mm
	



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## Low Power Voltage Detector

<b>正常 包装 流程</b>	1. 产品标签贴在卷盘正面，标签位置如下。	2. 载带在卷盘中的位置（载带定位孔朝卷盘反面一侧）。	3. 整卷编带完成，用 15cm 纸胶带将尾端贴合。	4. 装入屏蔽袋进行抽真空。真空压力-0.065MPa	5. 每 10 盘装入一个内盒。
					
	6. 内盒用透明胶带封口，标签贴在左上角位置。	7. 每 4 个内盒装入一个外箱，透明胶封口，标签贴在左上角位置。	8. 每个外箱不足 4 个内盒时用空内盒填充。		
					
<b>产品 特殊 说明</b>	<b>1. 尾数：</b> 尾数产品全部编带，用 Reel 盘包装。		<b>2. 并批：</b> a>同一客户、同一封装形式、同一产品型号。 b>并批卷，每卷最多合并不超过五个批次产品。 c>并批内盒，每内盒最多合并不超过十个批次产品。		<b>3. 不良品：</b> a> 不良品用红色自封口袋包装。 b> 标签使用产品标签，并在空白位置标注“不良品”字样。 c> 不良品需单独包装，不可与良品装入同一内盒、同一外箱。

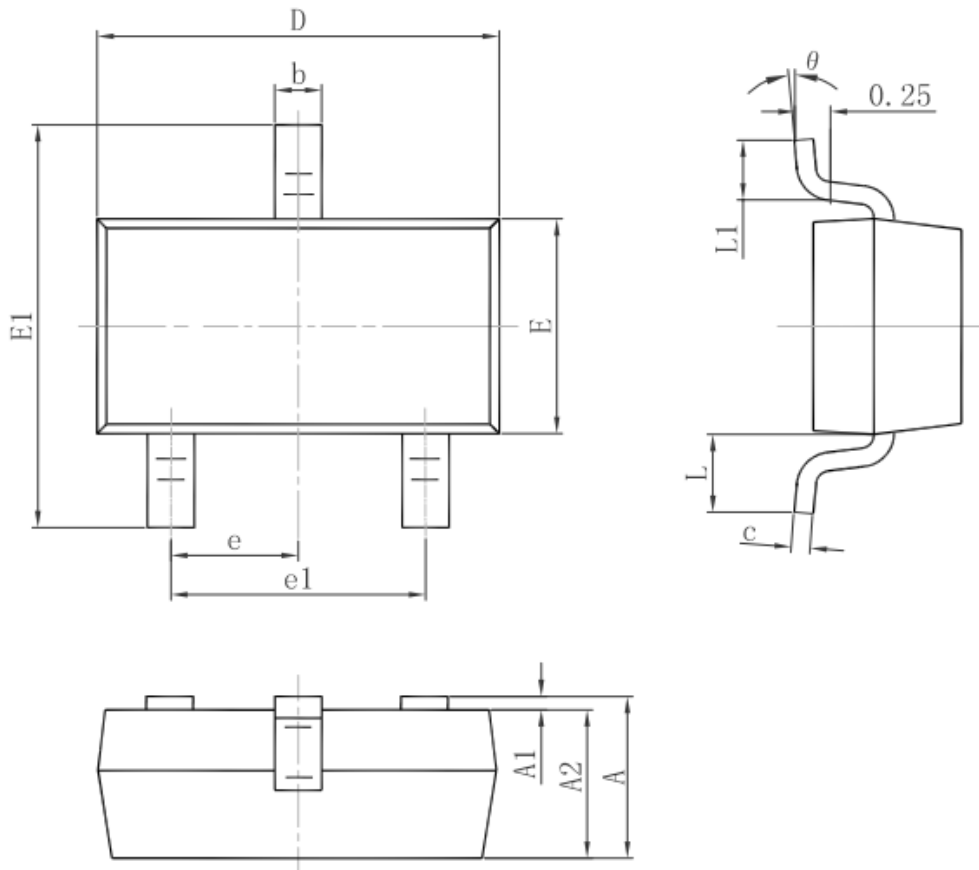


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## Low Power Voltage Detector

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### 3-pin SOT23 Outline Dimensions



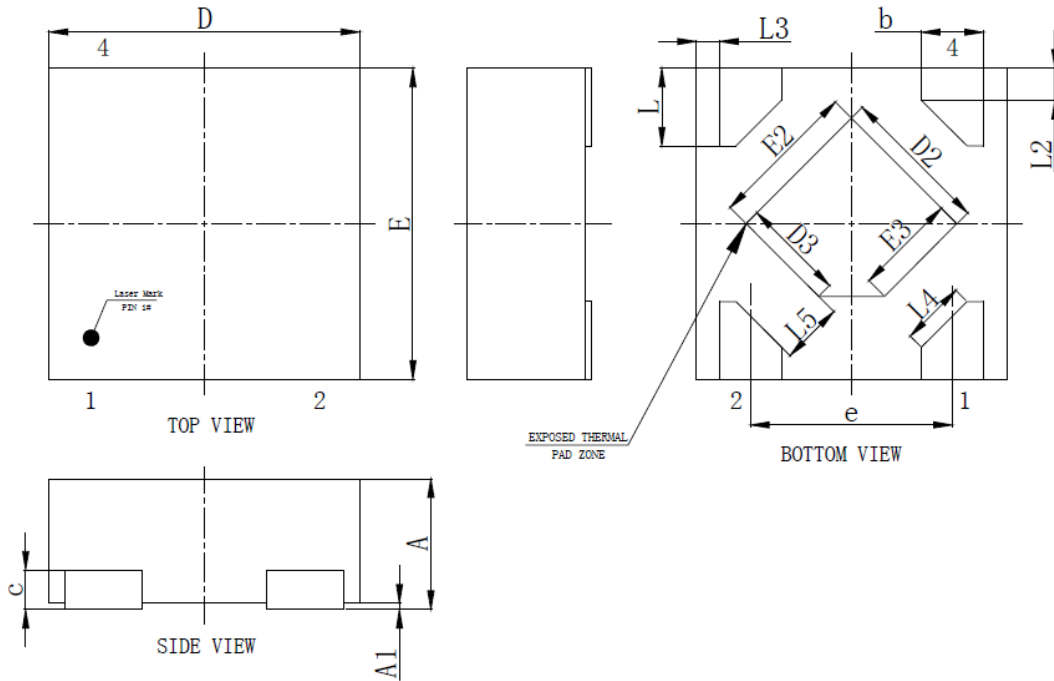
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
theta	0°	8°	0°	8°



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# TX61C series Low Power Voltage Detector

## DFN1\*1-4 Outline Dimensions



SYMBOL	MILLIMETER		
	MIN	MID	MAX
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	0.127REF		
D	0.95	1.00	1.05
D2	0.38	0.48	0.58
D3	0.23	0.33	0.43
e	0.65BSC		
E	0.95	1.00	1.05
E2	0.38	0.48	0.58
E3	0.23	0.33	0.43
L	0.20	0.25	0.30
L2	0.103REF		
L3	0.075REF		
L4	0.208REF		
L5	0.200REF		



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说明书更改说明:

版本	操作者	日期	更改内容	更改来源
1.2	郭玲博	2019-3-28	精度范围以 2.5V 划分, 2.5V 以下是 $\pm 50\text{mV}$ , 2.5V 以上是 $\pm 2\%$	测试说明。